AMENDMENTS TO THE DRAWINGS

Attached hereto are five (5) sheets of corrected formal drawings that comply with the provisions of 37 C.F.R. § 1.84. The corrected formal drawings incorporate the following drawing changes:

In Figs. 4-8, the legend "VB" has been added, and Figs. 5 and 6 have been amended to correspond to the description on page 2, lines 15-17, wherein "the gate clock signal CPV does not generate the start vertical signals STV1 and STV2 until after the vertical blank period VB (v-blank) of the data enable signal DE..."

It is respectfully requested that the corrected formal drawings be approved and made a part of the record of the above-identified application.

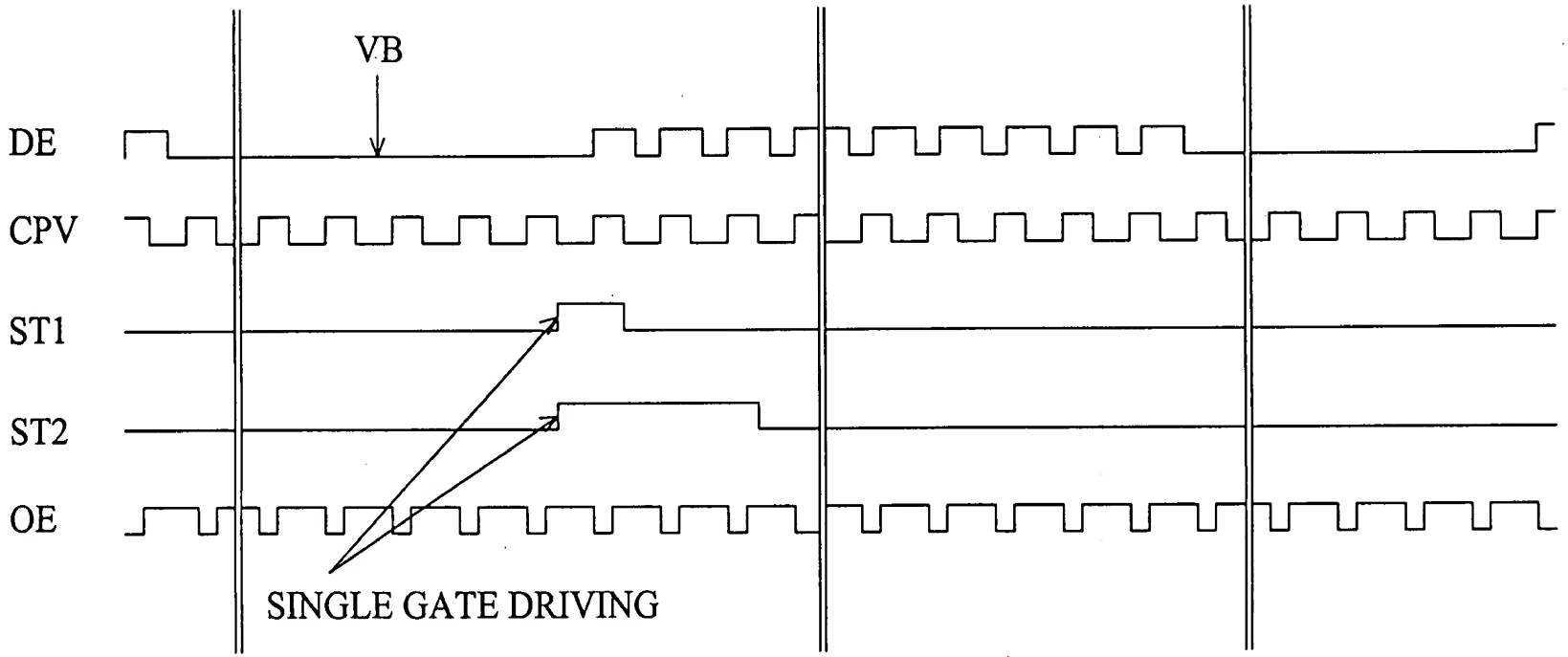

FIG. 4 (PRIOR ART)

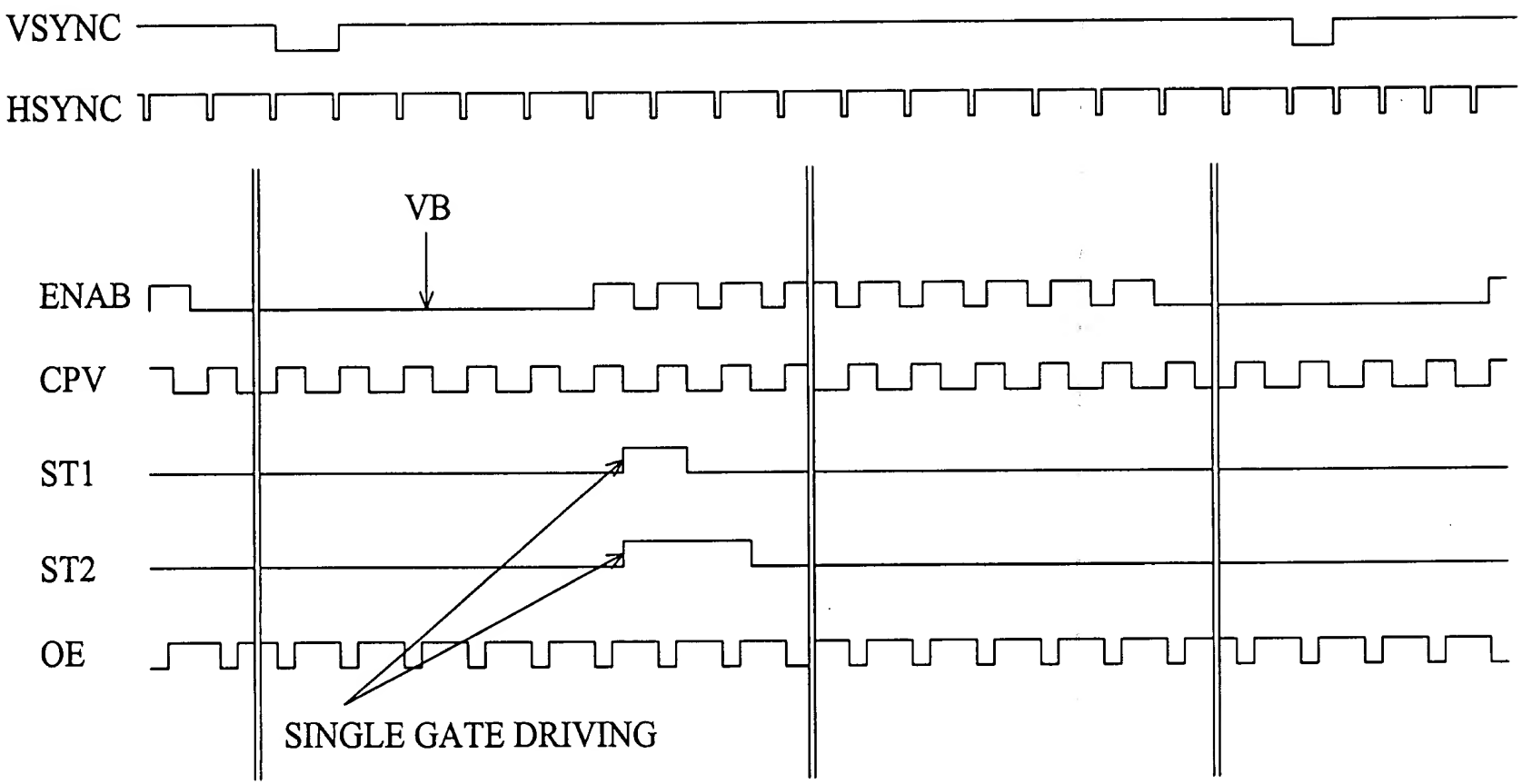

FIG. 5 (PRIOR ART)

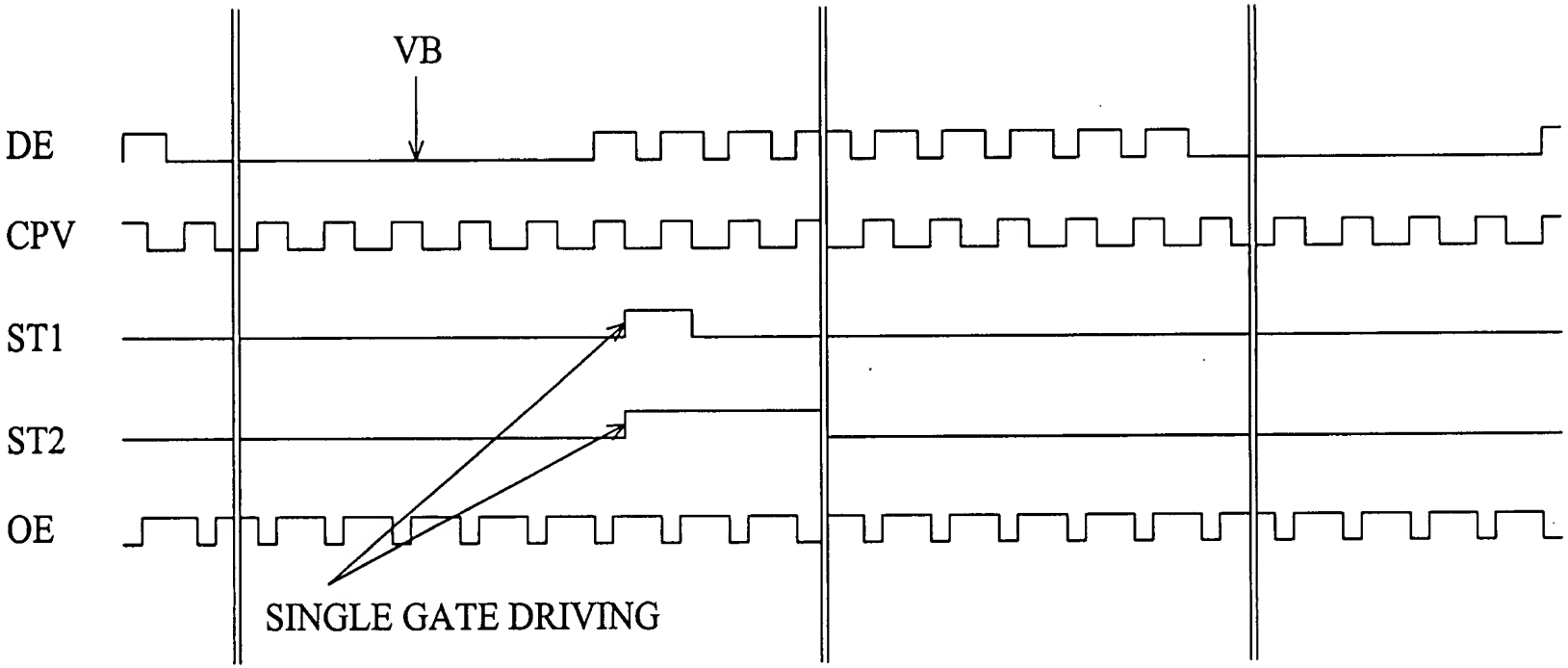

FIG. 6 (PRIOR ART)

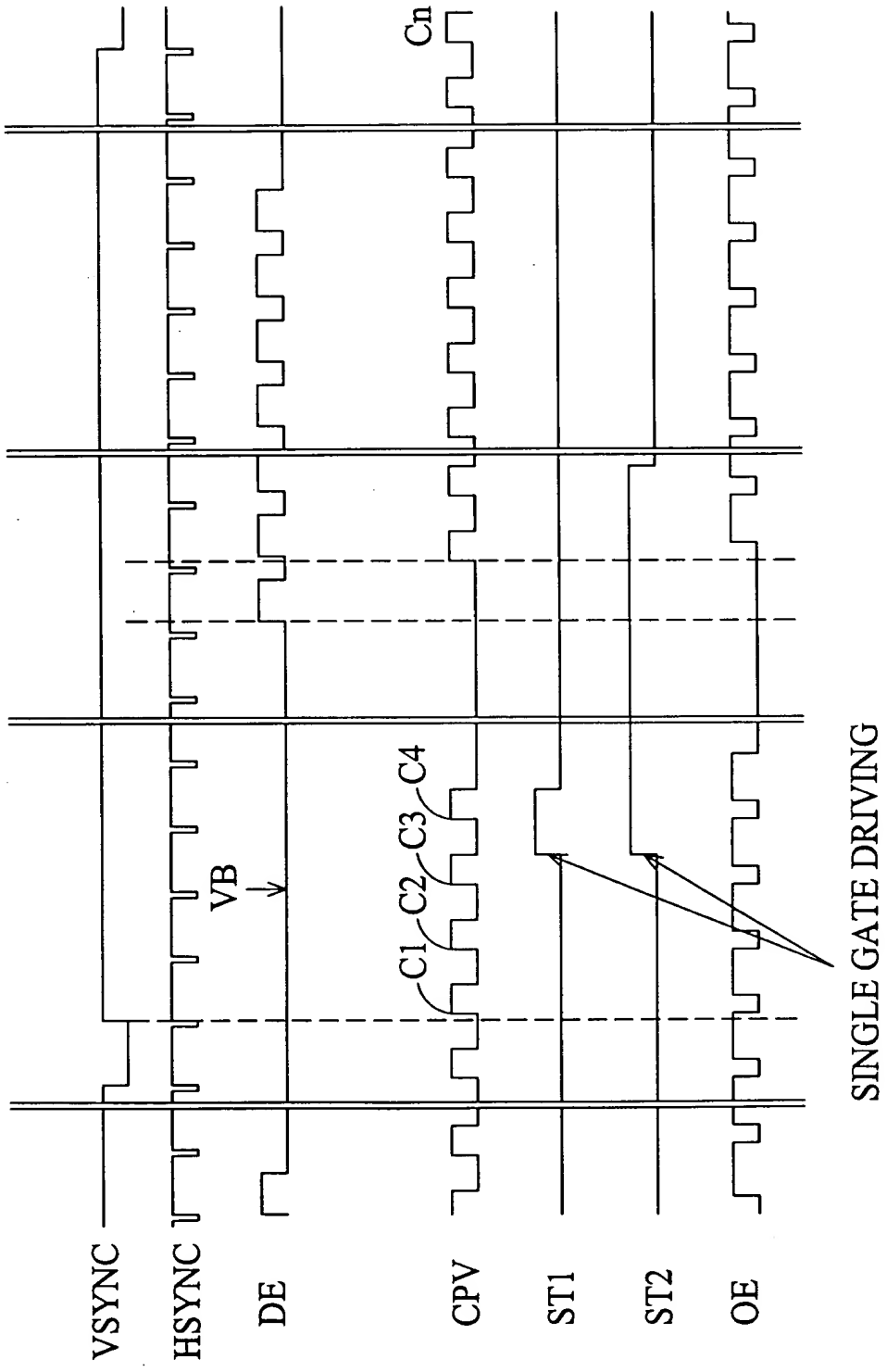

FIG. 7

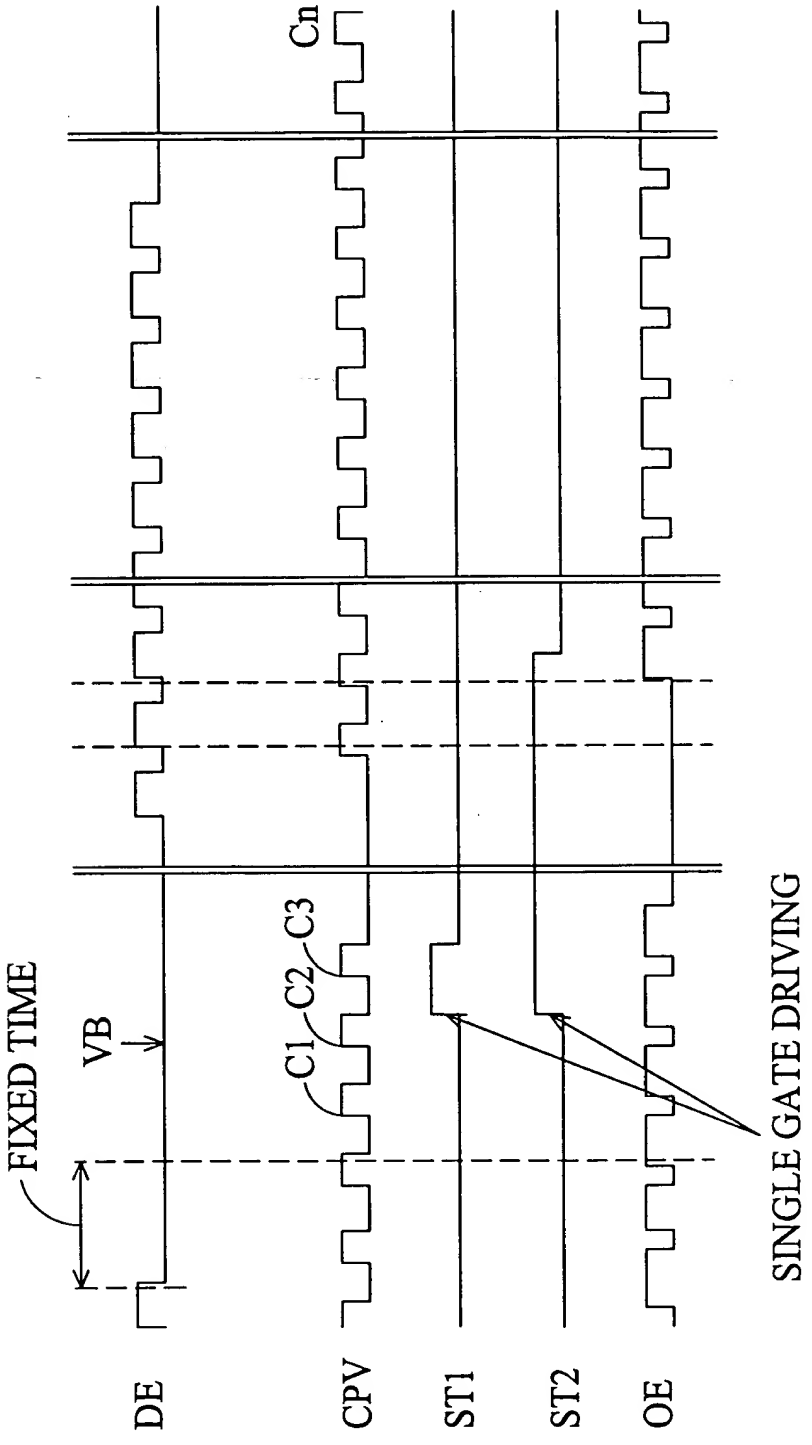

FIG. 8